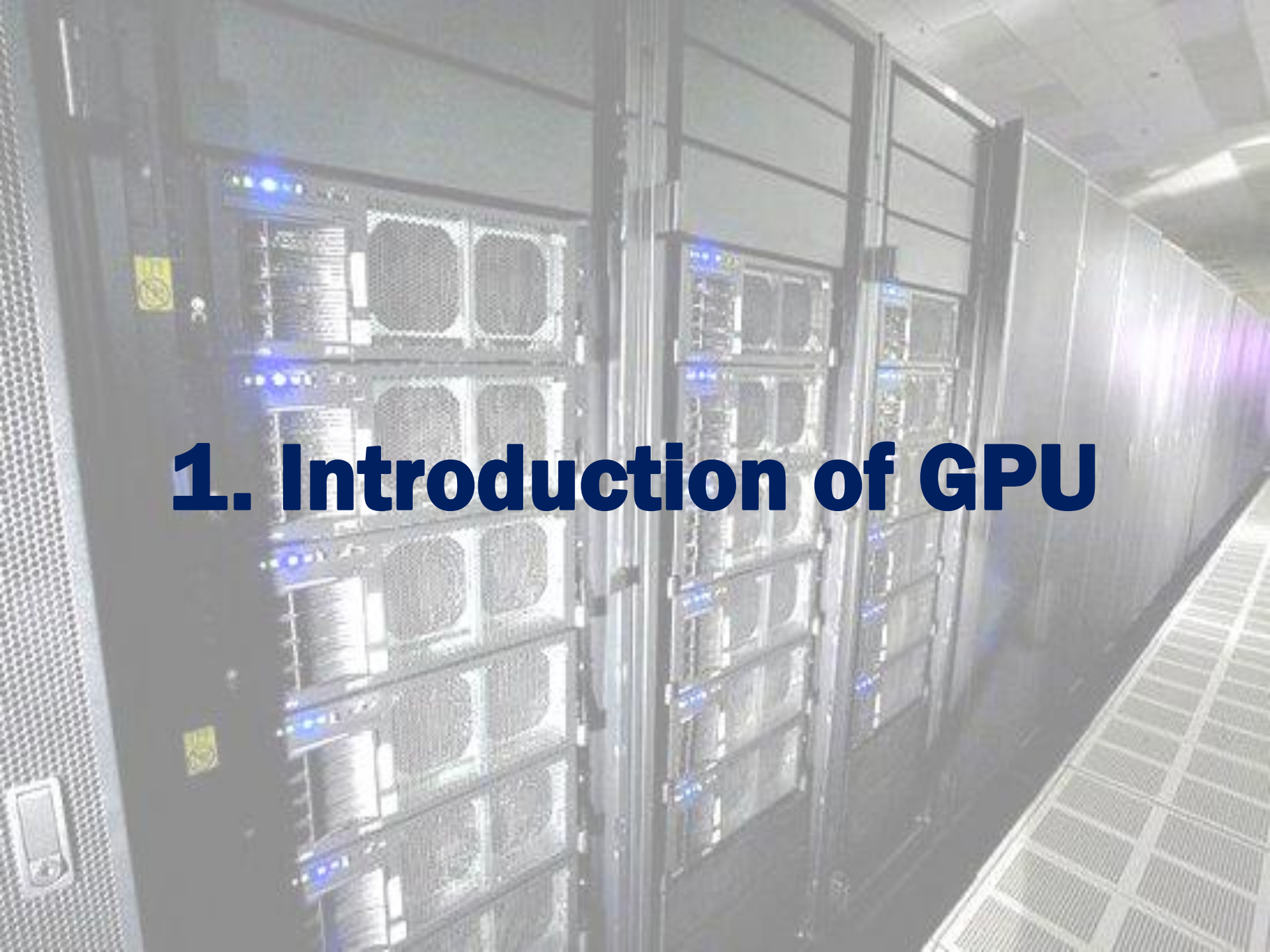
Parallelization Algorithm for Turbo Decoding and Its Implementation on GPU for SDR-based LTE System

Saehee bang

School of Electronics and Computer Engineering, Hanyang University
17 Haengdang-Dong, Seongdong-Gu, Seoul 133-791, Korea
Tel : 82-2-2299-6267, Fax : 82-2-2299-6263
E-mail : *say_0618@dsplab.hanyang.ac.kr*

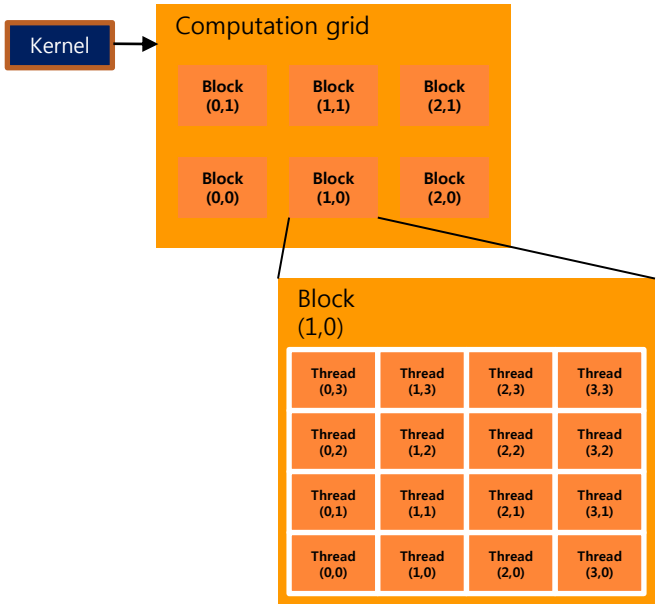
Contents



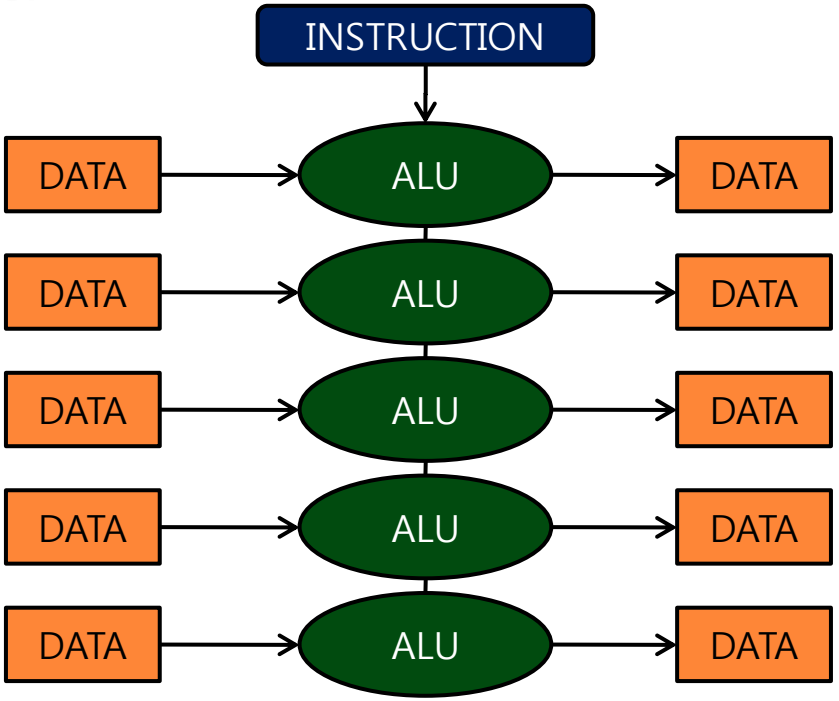
1. Introduction of GPU

Introduction of GPU – *Structure of GPU*

- Graphics Processing Unit (GPU)
- Single Instruction Multiple Data(SIMD)
- The GPU is massively parallel processor
- Kernel
  - A function compiled for Device

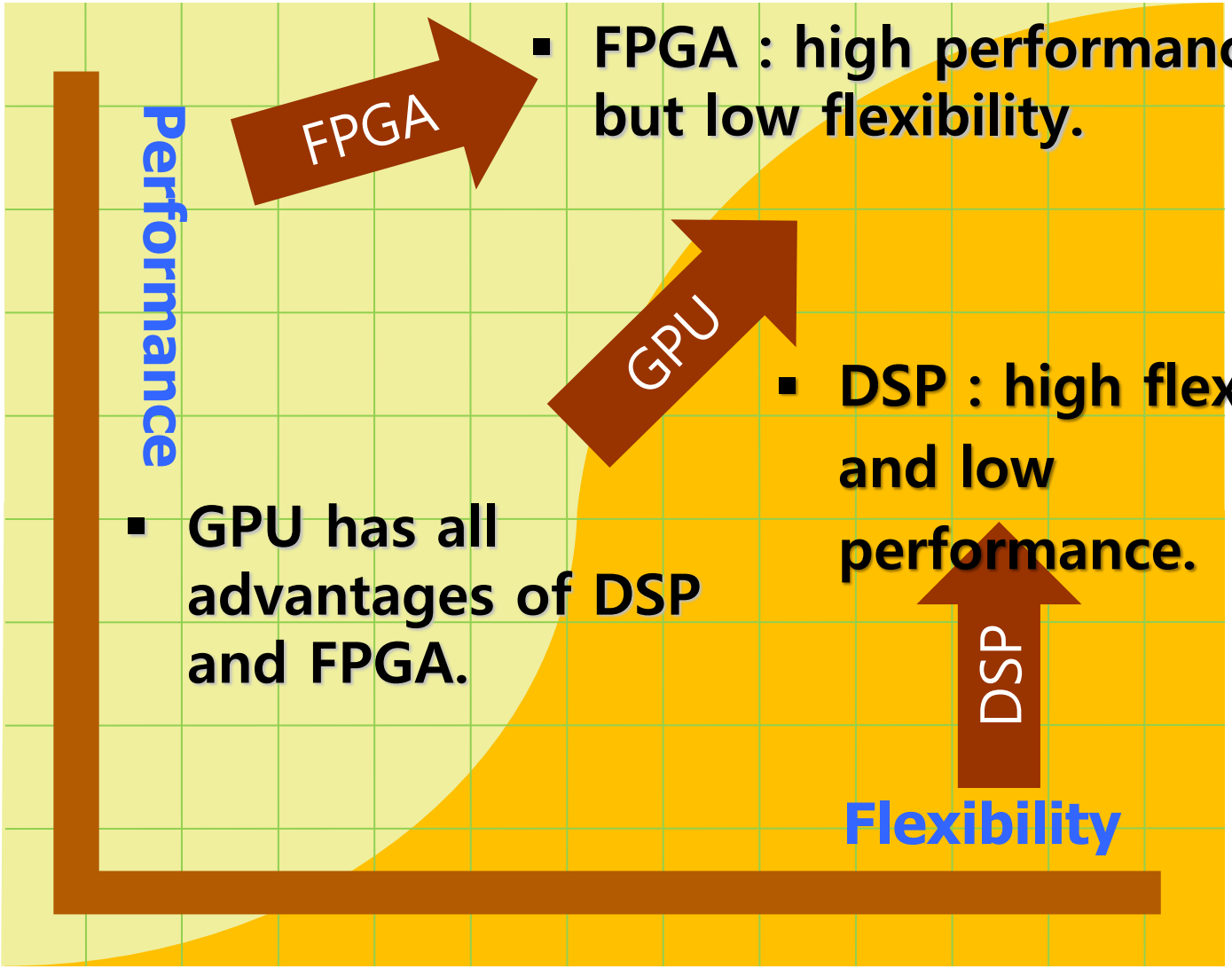


<Structure of CUDA Memory>



<SIMD processor architecture>

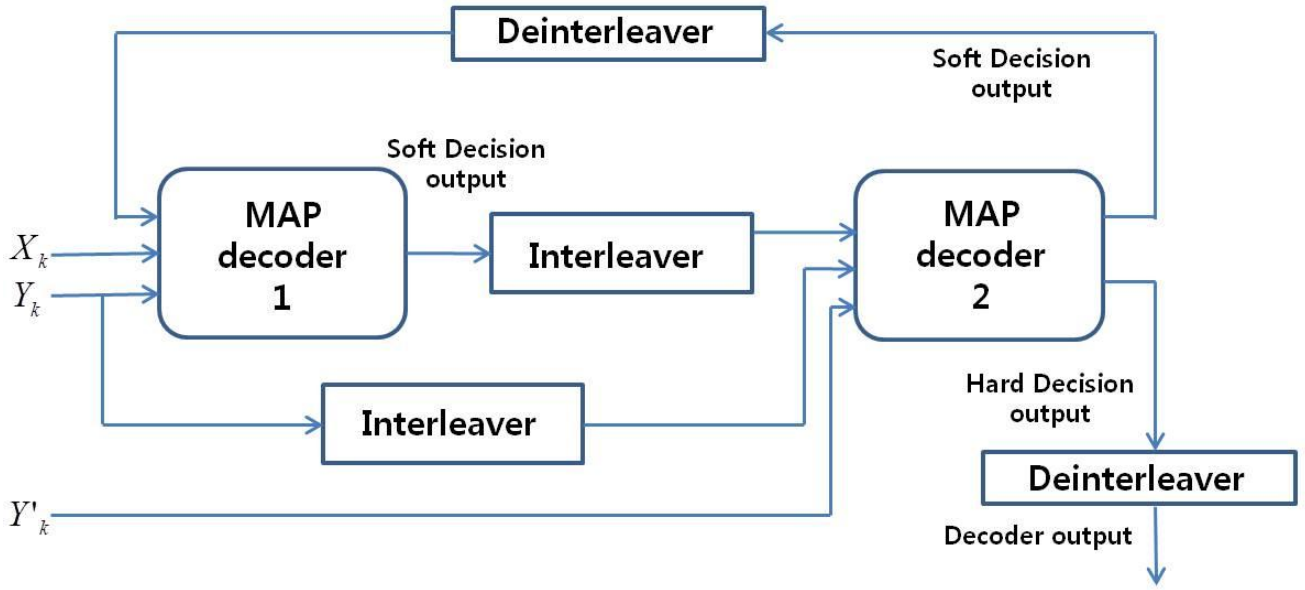
Introduction of GPU – *GPU vs DSP vs FPGA*



2. Implemented System

Implemented System – *turbo coding parallelization*

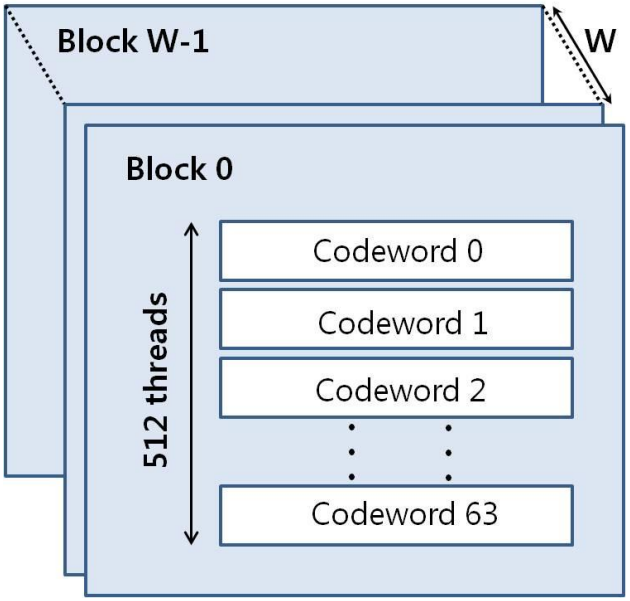
- **Block diagram of Turbo Decoder Architecture**
- **The parallelization of turbo coding algorithms appropriately for GPU**
  - **Interleaver / deinterleaver can be implemented simply**
  - **The procedure of computing the information sequence of each sub-block is dependent upon one another**



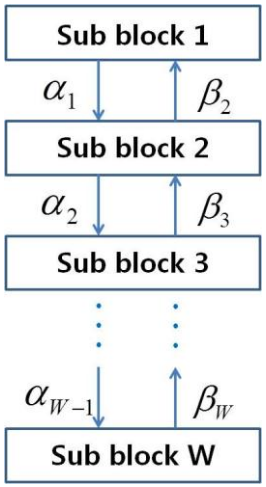
< Turbo Decoder Architecture >

Implemented System – *turbo coding parallelization*

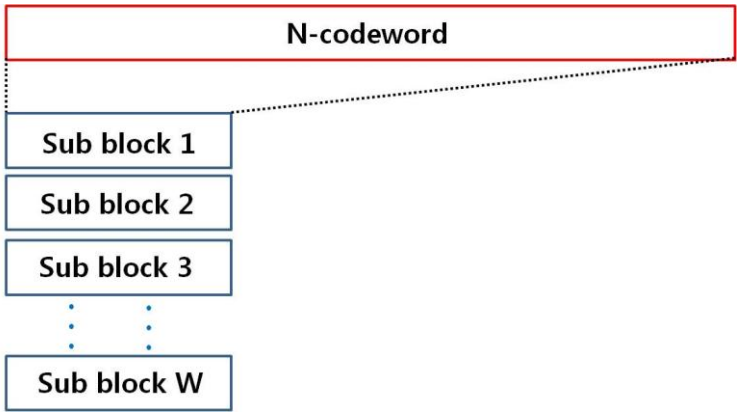
- **The parallelization of MAP decoder appropriately for the SIMD architecture**



<Operational architecture of GPU parallelization for MAP decoder>



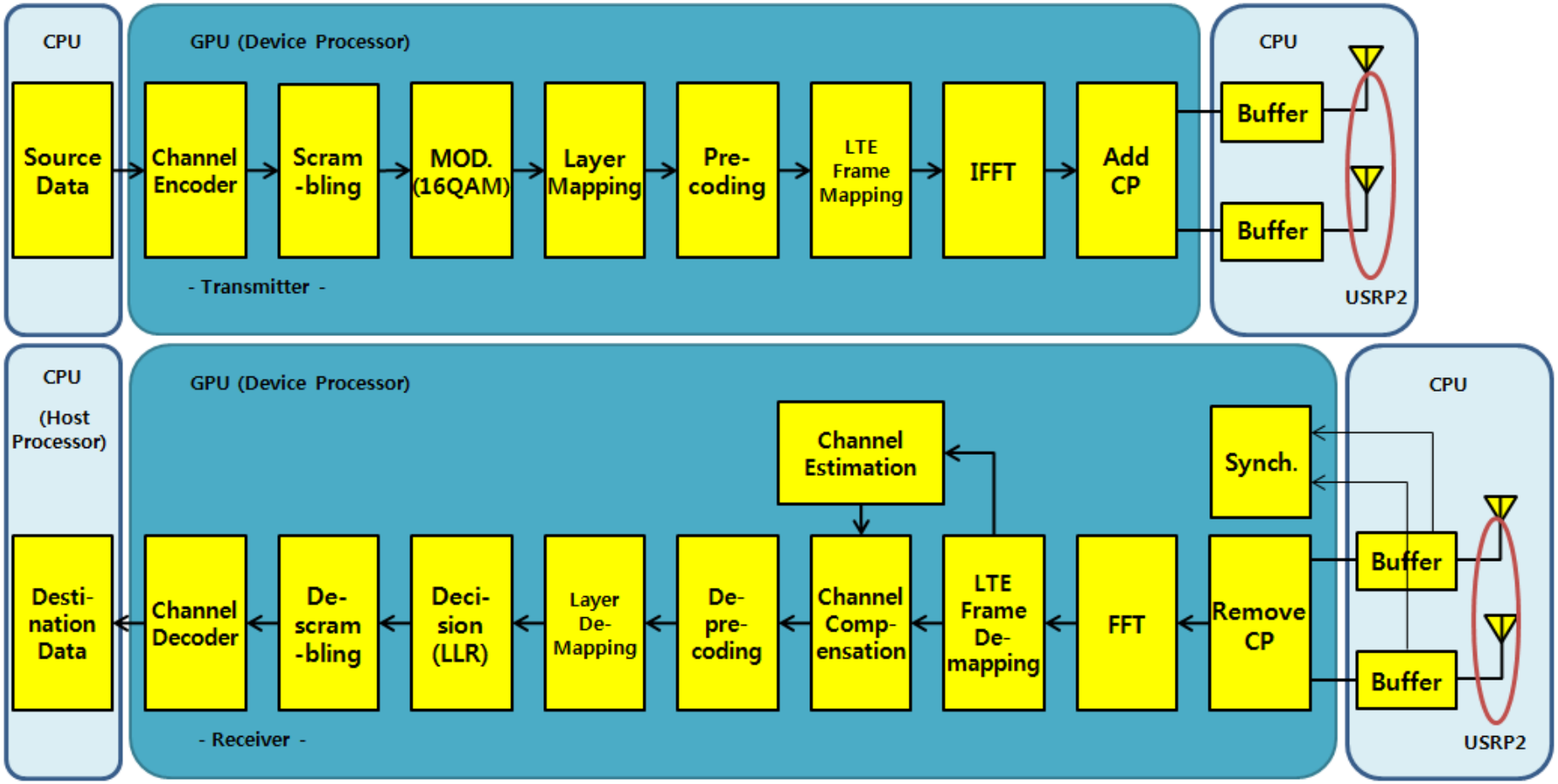
<Initial state value computation in the proposed algorithm>



<Decoding of N-code word with W partitioned sub-blocks>

Implemented System – *2x2 SM MIMO LTE system*

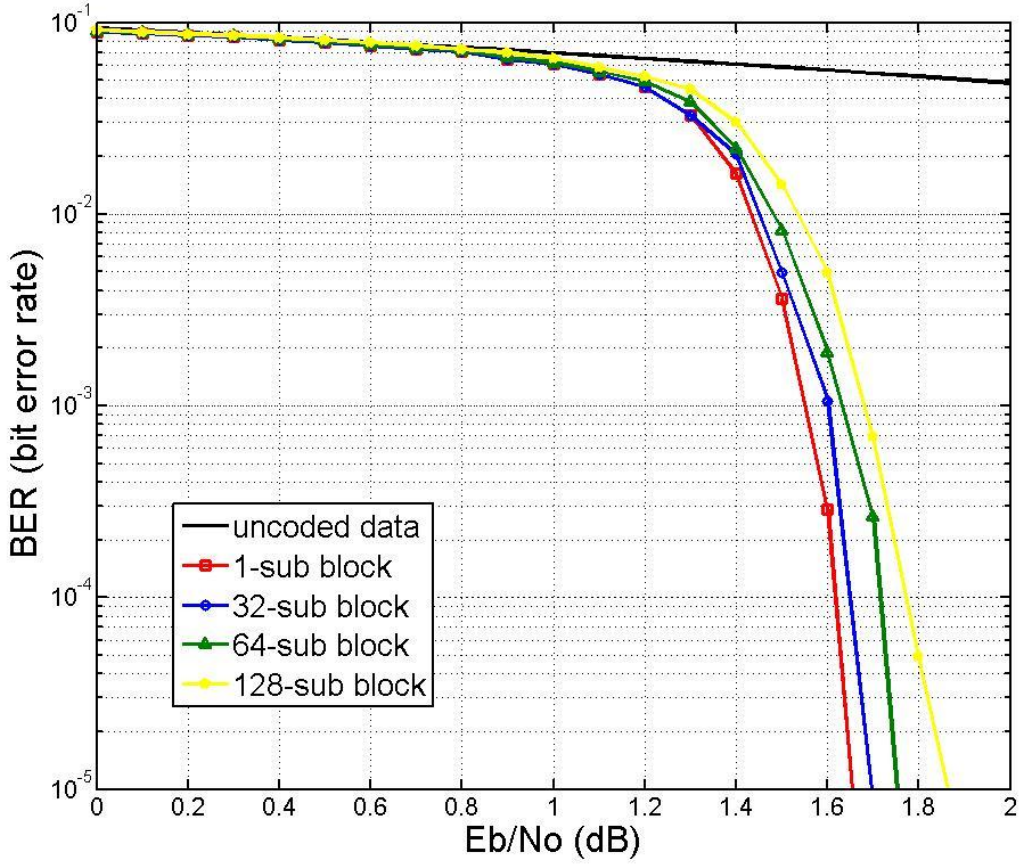
- **Block diagram of 2x2 SM MIMO LTE Downlink system**
- **The parallelization of signal processing algorithms appropriately for the SIMD architecture -** To use GPU and CPU resources effectively



3. Performance Analysis

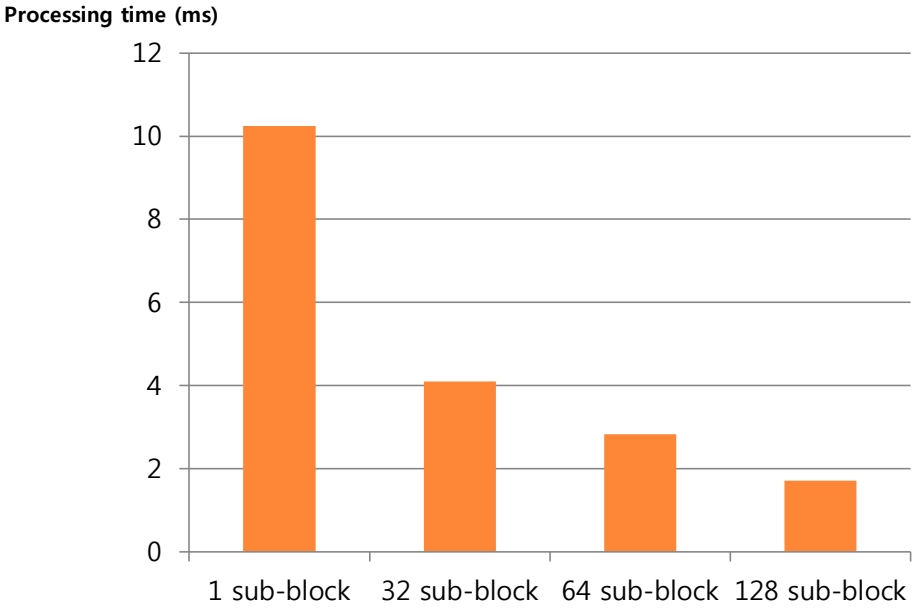
Performance Analysis – *BER Performance*

- **BER Performance of proposed method according to various number of sub-blocks.**



Performance Analysis – *Computation Time*

- **Profiler provided by NVIDIA**



Number of Sub-block	Total Processing Time for 6144 bits	Processing Speed
1	10.24ms	600Kbits/s
32	4.096ms	2.5Mbits/s
64	2.833ms	4Mbits/s
128	1.708ms	5Mbits/s

<Operation time taken for different number of sub-blocks>

Method	GPU time (μs)	%GPU time
Interleaver+deinterleaver	19.104	0.674
Memcpy	10.576	0.373
Other calculation	96.587	3.409
MAP decoder	2706.96	95.543
Total time	2833.227	100

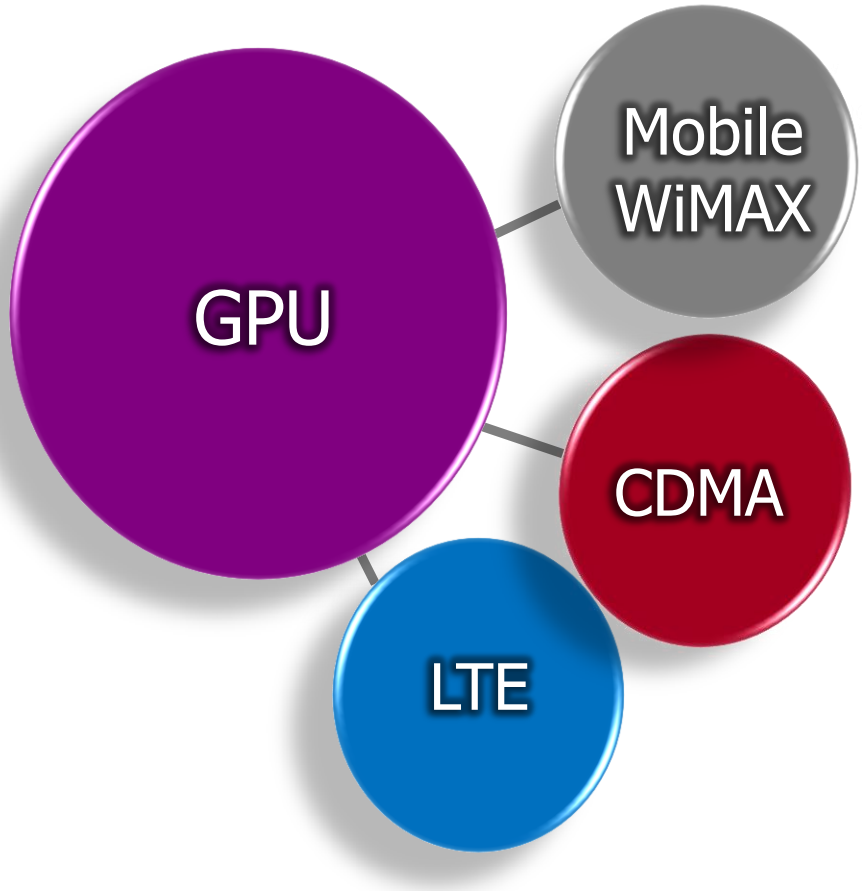
<64 sub-blocks>

Method	GPU time (μs)	%GPU time
Interleaver+deinterleaver	19.104	1.118
Memcpy	10.576	0.619
Other calculation	91.414	5.352
MAP decoder	1586.96	92.91
Total time	1708.054	100

<128 sub-blocks>

4. Conclusion

- GPU can be a solution because of its powerful computation capacity
- Also with the GPU, wireless communication systems can be implemented effectively for SDR.
- GPU can operate all waveform effectively.



Q / A

say_0618@dsplab.hanyang.ac.kr