DESIGN OF A PR NMD CHANNELIZER-BASED DOWN CONVERTER FOR RECEIVE UPLINK OF COMBINED 3GPP LTE AND UMTS RADIOS

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ABSTRACT

In this paper we present a novel application of perfect reconstruction (PR), non maximally decimated (NMD) polyphase channelizers whose assembly gives life to a compact Digital Down Converter (DDC) for combined Third Generation Partnership Protocol (3GPP), Long Term Evolution (LTE) radios and Universal Mobile Telecommunications System (UMTS) radios, which are Wideband Code Division Multiple Access (WCDMA) based. The design of the PR NMD analysis-synthesis chain has been optimized to maximize the performance according to the specific application scenario. The input sample rate and the desired output sample rates, drive us to select an 80-path, 40-to-1, PR NMD polyphase down converter channelizer to accomplish the pre-processing task of decomposing the complete frequency range and of aliasing all the spectral fragments to base-band while reducing the input sample rate. Because the input signal is real, the computation complexity of the 80 points Inverse Discrete Fourier Transform (IDFT), via Inverse Fast Fourier Transform (IFFT), is almost halved. A selector block is in charge of delivering the ports, which contain the fragments belonging to the same signal, to a proper PR 2-to-N ($N \in \{4,6,8\}$) up converter channelizer, which synthesizes them in base-band. A post-processing stage is required for filtering and frequency offset compensation.

1. INTRODUCTION

Standard 3GPP LTE digital front ends for receive uplink are generally implemented as cascade of half-band filters performing successive 2-to-1 down sampling [4]. A mixer, based on the assumption that the Intermediate Frequency (IF) is centered at one quarter sample rate is placed at the beginning of the down converting chain to shift the input spectrum to base-band before the sample rate reduction is performed (if this assumption is not true an alternative structure must be used). In this design the mixer operates at the input sample rate. A second stage of mixing has to be included in the design for multiple signal bandwidth configurations (e.g. four 5 MHz wide bandwidths or two 10 MHz wide bandwidths). A typical input sample rate of such a system is 307.2 Msps while standard output sampling rates are 7.38, 15.36, 23.04, 30.72 Msps [4]. The half-band filters are definitely a good option to consider when implementing a resampling with a factor of two because they require much less computational power (and thus less hardware) for a filter realization. This is due to the fact that every even indexed coefficient in the impulse response is zero except the center tap and even indexed coefficients are symmetric. However, the computation complexity of the half-band filter based DDC mainly depends on the received signal configuration and on the input/output sample rate requirements. Also, because the system is tailored to the input signal it lacks generality and cannot be utilized if the specifications change.

UMTS digital front end for receive uplink shares more than one characteristic with the LTE case. In particular the input sample rate, the desired output sample rates and the signal bandwidths are equal for the two systems. In the UMTS case the input sample rate must be wide enough to accommodate multiple WCDMA channels with some flexibility in carrier spacing. Because of the many similarities between the two scenarios, as for the LTE radios, current UMTS base station digital front ends for 3G communications are also implemented as cascades of half-band filters performing 2-to-1 successive down sampling. Mixers are included in the design for performing frequency translations of the input spectra in the multiband case [3]. It is clear that, as for the LTE case, the workload of such a system depends on the input sample rate and also, such a system lacks generality and cannot be utilized when different input or output specifications are given.

Notice that the main differences between 3GPP LTE and UMTS systems are the modulation format of the input signal and its shaping. However, these differences are not crucial and they do not affect the design of the PR NMD channelizer-based DDC. Therefore, in the following we will mainly refer to the LTE case specifying, when necessary, the differences with the WCDMA case.

The desire, common in the wireless industry, of achieving multi-purpose radios while maintaining good performance, low computation complexity, and cost reduction drives us to explore novel designs for digital down converter architectures. In this paper we present a DDC for combined 3GPP LTE and UMTS radios. The proposed architecture is based on polyphase filter banks. The need to accommodate a wide variety of input signals which are involved in the specific application case, drives us through a novel perfect reconstruction analysis-synthesis chain of NMD polyphase channelizers. The result is a customized solution which guarantees good performance and great efficiency.

The paper is organized in five main sections. In Section 1 the goals are specified and the proposed solution is anticipated. In Section 2 basics on PR NMD polyphase channelizers are provided and the reason for which they have been selected to serve our purposes is explained. In Section 3 the proposed architecture is presented while in Section 4 simulation results to demonstrate its correct functionality are given. The conclusions are provided in Section 5.

2. BACKGROUND

The perfect reconstruction property [1] can be achieved by properly designing the low-pass prototype filters of a cascade of polyphase analysis-synthesis (or synthesis-analysis) channelizers [2], [9] whose block diagrams, for clarity, are represented in figures 1 and 2 respectively.

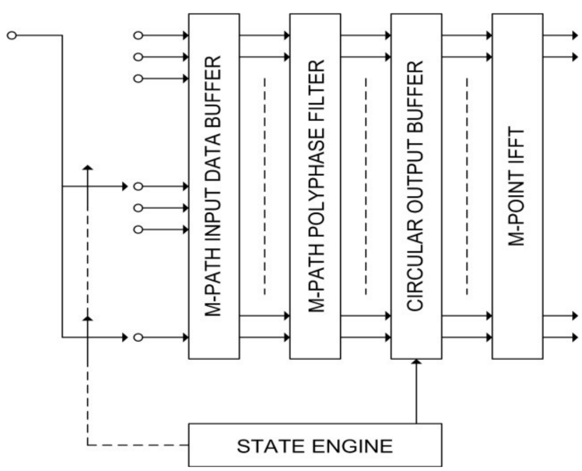

Figure 1: Polyphase Analysis Channelizer; Input Commutator and Data Buffer, M-Path Polyphase Partitioned Filter, Circular Data Buffer and M-Point IFFT.

Let us assume that the low-pass prototype filter is an M-times oversampled square-root Nyquist pulse. And this assumption is valid for both the analysis and synthesis block. If M is the number of arms of the filter bank (and it is also the number of IFFT points) in both the analysis and synthesis engines, the first tier analysis channelizer decomposes the input signal spectrum into M equally spaced, equal bandwidth sub-channels while performing $\frac{M}{2}:1$ down sampling of the input time series. The second tier synthesis channelizer re-assembles the M sub-channels while performing $1:\frac{M}{2}$ up sampling of its input time series. The result is a perfectly reconstructed version of the input signal at the output of the analysis-synthesis chain.

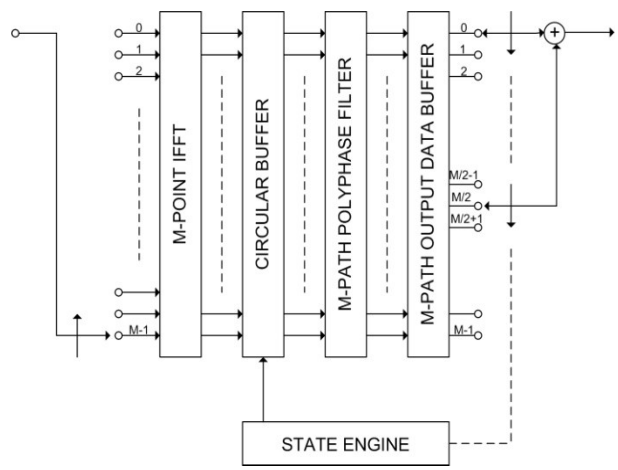

Figure 2: Polyphase Synthesis Channelizer; M-Point IFFT, Circular Buffer, M-Path Partitioned Filter, Output Data Buffer and Commutator.

The composition of those two engines finds its most efficient application in multiple bandwidth signal scenarios in which the individual bands composing the input spectrum are all simultaneously down converted and reassembled in base-band by multiple synthesis blocks. By modifying the structure of the channelizers (e.g. low-pass prototype filter, number of paths and commutator) interesting variations arise in which the PR property is preserved and the output sample rate can be customized according to the desired goals.

It is well known that the perfect reconstruction property is achieved when the composite response of the analysis and synthesis prototype low-pass filters form a Nyquist pulse [1], [2]. Let r(n) be the input sequence to the analysis channelizer, h(n) be the analysis channelizer prototype low-pass filter of length N_1; and g(n) be the synthesizer channelizer prototype low-pass filter of length N_2 where N_1 and N_2 are usually designed to be odd numbers. Then, the analysis filter $h_l(n)$ for the l^{th} path is written as $h_l(n)= h(n)e^{j\omega l n}$, where $\omega_l=2\pi l/M$ for l=0,1,…,M-1. Similarly, the l^{th} path synthesis filter is written as $g_l(n)= g(n)e^{j\omega l n}$. The signal at the output of the l^{th} analysis filter, denoted as $r_l(n)$, can be written as:

$$r_l(n) = \sum_{m=0}^{N_1-1} h_l(m)\, r(n-m) \qquad (1)$$

Signal $r_l(n)$ is then $\frac{M}{2}:1$ down-sampled and translated to the base-band. Let $\hat{r}_l(n)$ be the l^{th} down sampled base-band signal which is written as:

$$\hat{r}_l(n) = r_l\left(\frac{M}{2}n\right) e^{-j\omega_l \frac{M}{2}n} = r_l\left(\frac{M}{2}n\right) e^{-j\pi l n} =$$

$$\begin{cases} r_l\left(\frac{M}{2}n\right), & l \text{ is even} \\ r_l\left(\frac{M}{2}n\right)\cos(n\pi), & l \text{ is odd} \end{cases} \qquad (2)$$

We see from Eq.(2) that, after the $\frac{M}{2}:1$ down sampling, all the even indexed channels alias to base-band and all the odd indexed channels alias to half sample rate. Note that, the odd indexed channels can be translated to base-band trivially by multiplying with cos(nπ) after the down sampling process. At the output of the analysis channelizer, $\hat{r}_l(n)$ is $1:\frac{M}{2}$ zero packed and then fed into the l^{th} path synthesis filter. The $1:\frac{M}{2}$ zero packing process creates $\frac{M}{2}$ spectral copies and the synthesis filter $g_l(n)$ selects the copy centered on ω_l while rejecting other copies.

By following the same reasoning, and summing the previous result on all the paths, the overall PR channelizer output (analysis-synthesis chain) signal, y(n), can be expressed as:

$$y(n) = \sum_{l=1}^{M-1} r(n) * h_l(n) * g_l(n) =$$

$$= \sum_{l=1}^{M-1} \left\{ \left[\sum_{m=0}^{N_1-1} h(m) e^{j\omega_l m} g(n-m) e^{j\omega_l (n-m)} \right] * r(n) \right\}$$

$$= \sum_{l=1}^{M-1} \left[\left(h(n) * g(n) \right) e^{j\omega_l n} \right] * r(n)$$

$$= \sum_{l=1}^{M-1} h_{NYQ}(n) e^{j\omega_l n} * r(n) \qquad (3)$$

where $h_{NYQ}(n)=h(n)*g(n)$, is a Nyquist pulse.

Equation (3) explicitly shows that the PR channelizer implements a bank of M equally spaced Nyquist filters each centered on ω_l. The frequency responses of the adjacent Nyquist filters overlap at -6 dB (in power), and exhibit the even symmetry property with respect to the crossover point. Thus, we obtain the perfect reconstruction property whose analytical representation is shown in Eq. (4). A pictorial example of overlapping filter frequency responses which satisfies the PR property is shown in Figure 3 where the frequency axes has been resized to better visualize the -6dB crossover point.

$$\sum_{l=1}^{M-1} h_{NYQ}(n) e^{j\omega_l n} * r(n) = \sum_{l=1}^{M-1} Z_{\omega_l}(n) =$$
$$r(n)\delta\left(n - \frac{N_1+N_2}{2}\right) \qquad (4)$$

Notice that although an equality sign is used in Eq. (4), in practice the PR property is impaired by the filters' in-band ripple. From Eq.(4), we conclude that $Z_{\omega l}(n)$ is the shaped DFT evaluated on frequency ω_l at time instant n. The shaping pulse is $h_{NYQ}(n)$, which satisfies the PR property.

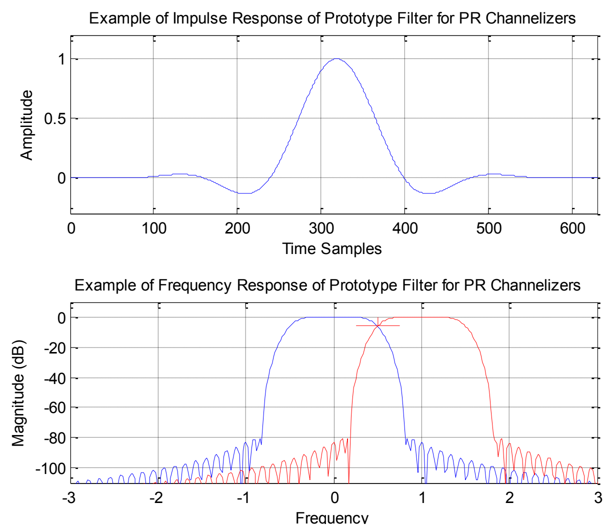

Figure 3: Example of Typical Impulse Response of Nyquist Low-Pass Prototype Filter (Upper Subplot) and Perfect Reconstruction Property of Analysis-Synthesis Chain (Lower Subplot).

3. PROPOSED DDC

Figure 4 shows the high level block diagram of the proposed DDC which is composed of two tiers NMD channelizers that create a PR analysis-synthesis chain. In the same figure are also indicated the lengths of the filters composing each path of the channelizers.

The optimum selection for the first tier channelizer has been an 80-path PR NMD down converter which performs 40-to-1 down sampling of the input time series. Its low-pass prototype filter is 800-tap long. This length guarantees 80dB out-of-band attenuation and an acceptable in-band ripple level [3],[4]. Because the total length of the filter has to be spread over all the paths, the partitioned filters in each arm of the bank are 10-tap long. This number gives a considerably small workload per path. The reason for using non maximally decimated channelizers is to avoid spectral folding problems which arise when the input signal is critically down sampled [2]. The selection of the channelizer size (number of paths as well as IFFT size) has been driven by the specifications given by this application case [3], [4]. In particular, it has been driven by the input sample rate and by the desired output sample rates according to the goals of minimizing the computation complexity and maximizing the performance as well as the flexibility of the design. Notice that the input sample rate of both 3GPP LTE and WCDMA signals is 307.20 Msps and, coincidentally, the desired output sample rates are: $f_s \in \{7.68, 15.36, 23.04, 30.72\}$ Msps. It is easy to recognize that the smaller of them, 7.68 Msps, is an integer sub-multiple of the input sample rate and, precisely, it is exactly 40 times smaller than 307.20 Msps. On the other side, 15.36 Msps, 23.04 Msps and 30.72 Msps are also integer multiples of 7.68 Msps. Thus the proposed architecture does avoid additional computation required by the inclusion of arbitrary interpolators in the design. In addition, it is well known [10] that when the input signal is real, the computation requirements of the IFFT are almost halved. Also, in this case, only half of the output ports of the channelizer need to be considered as valid inputs to the successive processing blocks of the chain.

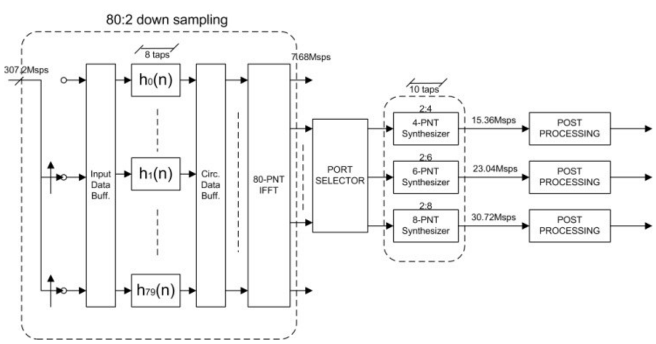

Figure 4: Proposed DDC; First tier 80-Path PR NMD Analysis Down Converter Channelizer, Second TierN-path PR Synthesis Up Converter Channelizers and Post Processing Blocks.

When the output ports of the first down converter channelizer, which contain spectral fragments belonging to the same signal, are delivered to the second tier channelizers, the spectral fragments are recomposed in base-band and the sample rate increases as desired. The desired output sample rates drive the selection of IFFT size of the small PR, 2-to-N, up converter channelizers. The bandwidth and the frequency location of the input signals also drive the selection of the proper synthesizer to whom the spectral fragments are delivered. The number of paths for the synthesizers have been selected to be $N \in \{4,6,8\}$. The lengths of the partitioned filters in each path is 10 taps which again guarantees the required out-of-band attenuation and in-band ripple level [3],[4] while giving a considerably small workload if compared to the standard existing DDC architectures which are based on cascades of half-band filters implemented in polyphase fashion.

A port selector, placed between the analysis and synthesis blocks, is in charge of delivering the outputs of the analysis channelizer to the appropriate up converter channelizers. We are assuming here perfect knowledge of the received signal bandwidths and frequency locations.

At the output of the small up converter channelizers the base-band shifted signals could require to be passed through post-processing blocks. An additional frequency offset correction could be needed for translating the spectra onto zero frequency. Remember that the down converter channelizer has the capability of shifting to DC only the signals which lie on exact multiples of the output sampling frequency [1], [2]. If a frequency offset is present it will be preserved during the processing. Also, a post-processing filtering stage could be required to reject undesired signal spectra which are so close to the signals of interest that the down converter channelizer by itself has not been able to filter them out. It is important to notice that the post-processing tasks are done at the end of the analysis-synthesis chain when the signal sample rate has already been reduced.

4. SIMULATION RESULTS

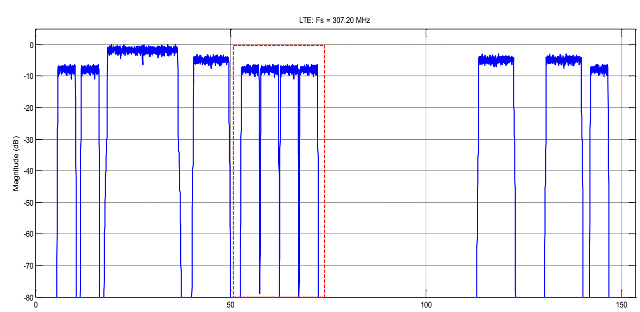

Figure 5: Input Spectrum to the Proposed PR Channelizer Based DDC.

Figure 5 shows the input spectrum to the DDC which is composed of multiple bands which are 5, 10 and 20 MHz wide. The four 5 MHz bands centered around 57.5 MHz, which are enclosed in the dotted red line, represent a typical 3GPP LTE signal. Those are the spectra that we want to recover at the output of the processing chain.

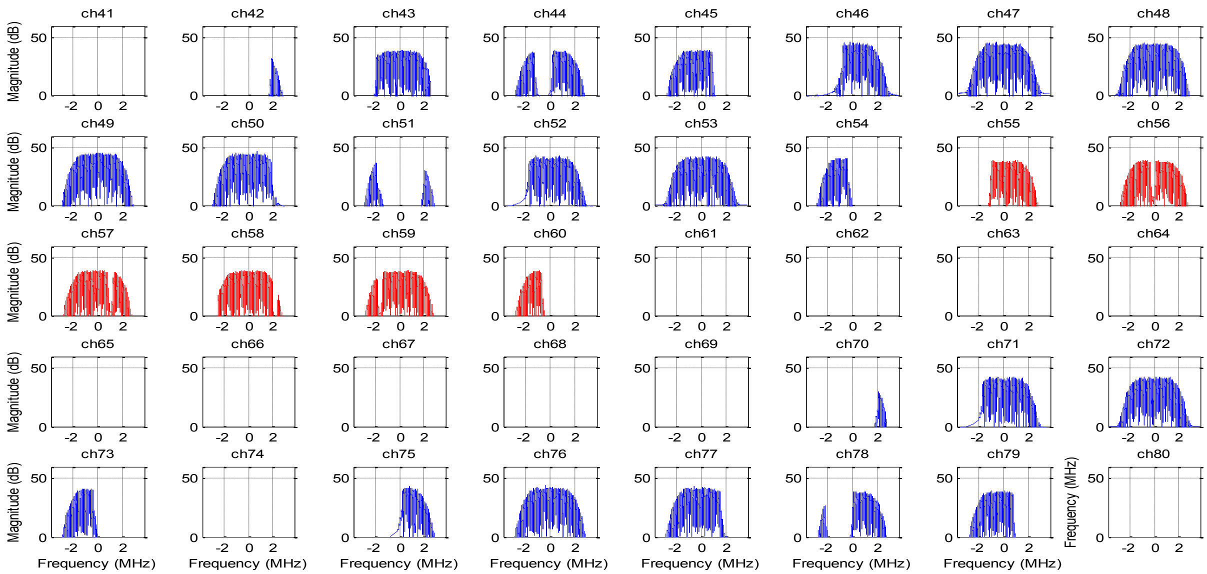

Figure 6: Output Spectrum of the 80-Path PR NMD Down Converter Channelizer.

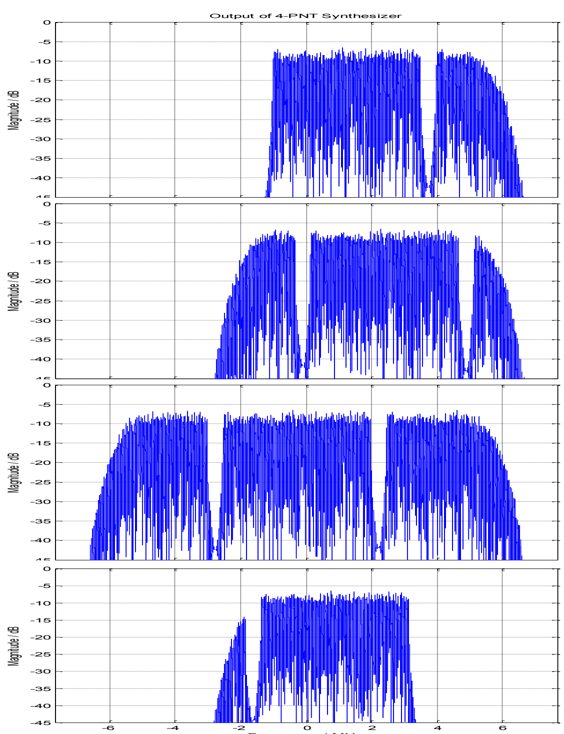

Figure 7: Output Spectra of the 4-Path PR NMD Up Converter Channelizer.

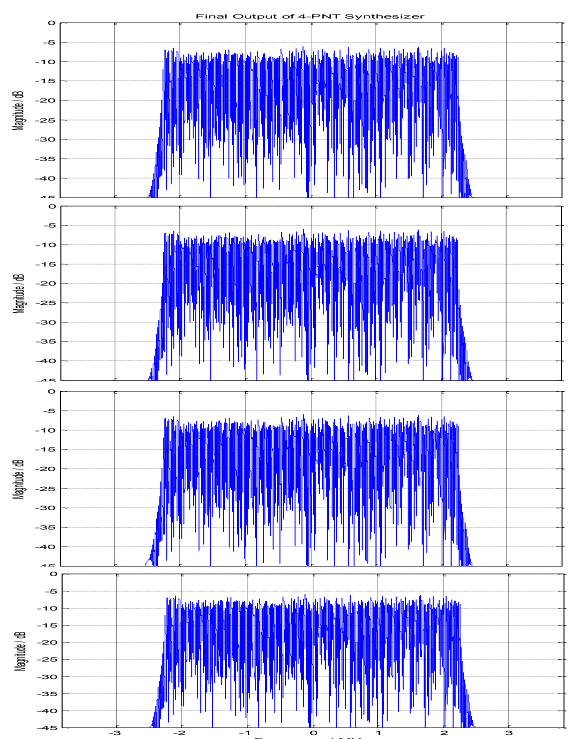

Figure 8: Output Spectra of the Post Processing Blocks.

The other signal bands have been introduced in the picture as interference signals which have been acquired by the analog Radio Frequency (RF) front end of the base station receiver and have to be rejected by the DDC. Such a spectrum has been generated for demonstrating the functionality of the proposed architecture in a dramatic case in which intensive use of post processing is required. The signals of interest have been generated as specified in section 5.6 of 3GPP TS 36.211 [8]. They are OFDM symbols with 512 IFFT points and 300 subcarriers to whom cyclic extension has been added.

Figure 6 shows the output of the first tier down converter channelizer. The red spectra are the desired ones. The blue spectra are the interferers we have to filter out. The rejection of these undesired signal bands is automatically done by using the proposed architecture and it does not cost any additional computation. By noticing that each subplot of Figure 6 represents an output port of the PR down converter channelizer we conclude that it is sufficient not to deliver the output ports which contain undesired signals to the up converter channelizers which are in charge of the signal recomposition and up sampling. Notice that only 40 of the total of 80 output channelizer ports have been plotted in Figure 6. In fact the input spectrum to the DDC is real and only half of the channelizer output ports are necessary to recover the desired signals. Also notice that the output sample rate is 7.68 Msps as desired.

In Figure 7 the four spectra at the output of the up converter synthesizers are shown. Because the desired bandwidths are 5 MHz wide, the output ports of the first tier channelizer have been delivered to a four points up converter. Given that the output sampling rate of the first tier down converter channelizer is 7.68 Msps, at the output of the second tier channelizer, which performs 1-to-2 up sampling, the signal sample rate is 15.36 Msps. In Figure 7 it is clearly visible that signal post processing is required for rejecting adjacent signal bands and for correcting the residual frequency offset which is a consequence of the arbitrary center frequency location of the input signals. Also a 2-to-1 down sampling stage has to be applied before delivering the final output signals to the digital back-end.

In Figure 8 the output of the post processing stages are shown. Even though the post processing filter is 144 taps long, because the post processing is performed at the output of the processing chain, its impact on the total workload is strongly reduced.

5. CONCLUDING REMARKS

In this paper we have presented a new application of polyphase channelizers. The desire of achieving DDCs for combined 3GPP LTE and UMTS base station radios has driven us to design a new PR NMD analysis-synthesis chain that minimizes the computation complexity and maximizes the performance. The structure we present here is the most efficient one between the many options we have tried.

Digital down converters for 3GPP LTE and WCDMA signals are traditionally implemented as cascades of half-band filters which make them signal dependent. The proposed design is signal independent and it has a competitive workload if compared to the traditional DDC architectures. The analysis channelizer in the proposed DDC is an 80-path PR NMD down converter which performs 40-to-1 down sampling of the input time series while the synthesizers are smaller up converter channelizers which perform 2-to-N up sampling of the input time series. They recompose the signal bands in base-band while adjusting their sample rate. A post processing block has been added to the design for frequency offset correction and filtering. Because the post processing happens at very low sample rate its impact on the overall computation complexity is minimal.

It is important to specify that the dimensionality of the channelizers have been selected according to the input and output sampling frequencies of typical LTE-GSM receivers thus they avoid the utilization of arbitrary interpolators which will require additional computations.

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